

CLAIMS

1. A method of generating a phase error signal from a reference signal and a feedback signal, the method comprising the steps of:

5 receiving a reference signal and a feedback signal using an input circuit;

generating a phase error signal using a phase error detector circuit; and

10 resetting the input circuit and, after a delay, resetting the phase error detector circuit.

2. The method of claim 1 wherein the amount of delay is variable and is used to select an appropriate amount of delay to reduce a dead zone to less than one picosecond.

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3. The method of claim 2 wherein the amount of delay is variable from 5% to 25% of the period of the reference signal.

4. The method of claim 1 wherein the amount of delay is temporarily set at an amount appropriate to reduce the dead zone to less than one picosecond.

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5. The method of claim 4 wherein the amount of delay is temporarily set at a value between 5% and 25% of the period of the reference signal.

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6. A method of generating a phase error signal from a reference signal and a feedback signal, the method comprising the steps of:

30 setting a first and a second latch circuit after

receiving the reference signal and the feedback signal, respectively, and generating a latched reference signal and a latched feedback signal, respectively, until a first reset signal is received;

5 generating a derived reference signal and a derived feedback signal, based on the reference signal and the feedback signal, respectively, using a first and second dynamic AND circuit, respectively, until a second reset signal is received;

10 receiving the derived reference signal and the derived feedback signal in a reset circuit and generating the first reset signal and, after a delay, generating the second reset signal; and

15 generating a pulse, in a pulse shaping circuit, based on the derived reference signal and the derived feedback signal, with pulse width proportional to the delay between the derived reference signal and the derived feedback signal.

7. The method of claim 6 wherein the amount of delay is variable and is used to select an appropriate amount of delay to reduce a dead zone to less than one picosecond.

8. The method of claim 7 wherein the amount of delay is variable from 5% to 25% of the period of the reference signal.

25 9. The method of claim 6 wherein the amount of delay is temporarily set at an amount appropriate to reduce the dead zone to less than one picosecond.

10. The method of claim 9 wherein the amount of delay is temporarily set at a value between 5% and 25% of the period of the reference signal.

5 11. An apparatus for generating a phase error signal from a reference signal and a feedback signal, the apparatus comprising:

means for setting a first and second latch after receiving the reference signal and the feedback signal,
10 respectively, and for generating a latched reference signal and a latched feedback signal, respectively, until a first reset signal is received;

means for generating a derived reference signal and a derived feedback signal, based on the reference signal and
15 feedback signal, respectively, until a second reset signal is received;

means for receiving the derived reference signal and the derived feedback signal in a reset circuit, for generating the first reset signal, and after a delay, for generating the
20 second reset signal; and

means for receiving the derived reference signal and the derived feedback signal in a pulse shaping circuit, and for generating a pulse with width proportional to the delay between the derived reference signal and the derived feedback
25 signal.

12. The apparatus of claim 11 wherein the amount of delay is variable relative to the period of the reference signal and is used to select an amount of delay appropriate to
30 reduce the dead zone to less than one picosecond.

13. The apparatus of claim 12 wherein the amount of delay is variable from 5% to 25% of the period of the reference signal.

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14. The apparatus of claim 11 wherein the amount of delay is temporarily set at an amount appropriate to reduce the dead zone to less than one picosecond.

10 15. The method of claim 14 wherein the amount of delay is temporarily set at a value between 5% and 25% of the period of the reference signal.

16. A computer program product for generating a phase error signal from a reference signal and a feedback signal, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer program code for setting a first and second latch after receiving the reference signal and the feedback signal, respectively, and for generating a latched reference signal and a latched feedback signal, respectively, until a first reset signal is received;

computer program code for generating a derived reference signal and a derived feedback signal, based on the reference signal and the feedback signal, respectively, until a second reset signal is received;

computer program code for receiving the derived reference signal and the derived feedback signal, for generating the first reset signal, and after a delay proportional to the period of the reference signal, for generating the second

reset signal; and

computer program code for receiving the derived reference signal and the derived feedback signal in a pulse shaping circuit, and for generating a pulse that has a width
5 proportional to the delay between the derived reference signal and the derived feedback signal.

17. The computer program code of claim 16 wherein the amount of delay is variable and is used to select an
10 appropriate amount of delay to reduce the dead zone to less than one picosecond.

18. The computer program code of claim 17 wherein the amount of delay is variable from 5% to 25% of the period of
15 the reference signal.

19. The computer program code of claim 16 wherein the amount of delay is temporarily set at an amount appropriate to reduce the dead zone to less than one picosecond.
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20. The computer program code of claim 19 wherein the amount of delay is temporarily set at a value between 5% and 25% of the period of the reference signal.

25 21. A phase/frequency detector circuit, comprising:
a first latch circuit configured for receiving a reference signal and a first reset signal, and for generating a latched reference signal;
a second latch circuit configured for receiving a
30 feedback signal and a second reset signal, and for generating

a latched feedback signal;

a first dynamic AND circuit configured for receiving the reference signal, a first NOR signal and a second reset signal, and for generating a derived reference signal;

5 a second dynamic AND circuit configured for receiving the feedback signal, a second NOR signal and the second reset signal, and for generating a derived reference signal;

a first NOR circuit coupled to the first latch circuit for receiving the latched reference signal and coupled to the first dynamic AND circuit for receiving the derived reference
10 signal, and for generating the first NOR signal;

a second NOR circuit coupled to the second latch circuit for receiving the latched feedback signal and coupled to the second dynamic AND circuit for receiving the derived feedback
15 signal, and for generating the second NOR signal;

a reset circuit coupled to the first and second dynamic AND circuits configured for receiving the derived reference signal and the derived feedback signal, respectively, and coupled to the first and second latch circuits for providing
20 the first reset signal, and further coupled to the first and second dynamic AND circuits for providing a second reset signal, after a delay proportional to the period of the reference signal; and

a pulse shaping circuit coupled to the first and second
25 dynamic AND circuits configured for receiving the derived reference signal and the derived feedback signal, respectively, and generating a pulse that has a width proportional to the delay between the derived reference signal and the derived feedback signal.

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22. The phase/frequency detector circuit of claim 21 wherein the amount of delay is variable and is used to select an appropriate amount of delay to reduce the dead zone to less than one picosecond.

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23. The phase/frequency detector circuit of claim 22 wherein the amount of delay is variable from 5% to 25% of the period of the reference signal.

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24. The phase/frequency detector circuit of claim 21 wherein the amount of delay is temporarily set at an amount appropriate to reduce the dead zone to less than one picosecond.

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25. The phase/frequency detector circuit of claim 24 wherein the amount of delay is temporarily set at a value between 5% and 25% of the period of the reference signal.